microns and never that the specification discloses the range of 0.5 to 1.0 microns. That is incorrect.

On page 10, lines 20-21, at the first mention of the sidewall spacer, a thickness of preferably 0.5 to 1.0 um is clearly disclosed. Furthermore, on page 13, lines 12-16, in characterizing the thickness of the vertical layer, two example values of sidewall spacer thickness, 1 um and 0.5 um, are used to show what could be expected for the thickness of the vertical layer of the substrate.

not true claims 37, 38 is for 2nd emb., p. 10 is for the 1st emb.

The disclosure on page 16 that the Examiner cites as ground for this rejection deals with an alternative embodiment shown in Fig. 14-20 applicable to 5-6 um first trench depth vs. ~<2 um depth in the embodiment shown in Fig. 4. The Fig. 14-20 embodiment also contains two different gate oxide thicknesses where substantial erosion of the spacer takes place when the first gate oxide (160A) is removed from the top portion of the first trench. To allow for such erosion during the process, a thicker spacer is recommended. Again, these numbers are given as examples and not as absolute limits depending on the etch rate of the spacer in the gate oxide removal etchant.

Accordingly, the specification clearly supports spacer thicknesses in the range of 0.5-1 micron.

The Examiner rejected claims 23, 30-39 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention, citing specific objections to claims 34, 31 and 36.

Claim 34 is amended to remove the § 112(2) objections. Line 6 now refers to "first predetermined depth," which is shown in Fig. 5 as depth 56. The phrase "vertically-oriented layer of the semiconductor substrate" in line 15 itself makes clear that it is a part of the substrate, and lines 20-21 further recite that the (lower) first vertical layer portion (90) is "contiguous with the body layer" (26") (See Fig. 11). Line 19 is amended to refer to "the

vertically-oriented layer on a side of the second trench." Line 24 is amended to recite "said second polarity dopant." Line 34 is amended to recite "PN junction."

Claim 31 is amended to recite "said second trench" in line 3; line 6 is amended to refer to "opposite sides of the second trench."

Claim 36 is amended to make clear that the vertically-oriented layers are on each side of the second trench, and to more clearly relate the "vertically-oriented insulative layer" to that recited in claim 35, from which claim 36 depends; and to change "sidewall spacers" to "vertically-oriented insulative layers" to be consistent.

Claims 23, 30-39 should now be allowable under § 112.

Response to § 103 Rejection

A new claim 40 is added, which presents in independent form the subject matter of claim 36, with details regarding doping omitted for clarity. This claim specifically differentiates the properties of the spacers (44) and isolation layer (68) over Sakamoto. Sakamoto's spacer is a composite of thermally grown oxide (9) and a deposited insulator (13) in Figs. 2c-2d, anisotropically dry etched to leave a portion of (13) on the sidewall of (9), or completely thermally grown as in Fig. 4c or completely deposited and contiguous film over a tungsten gate and etched back to a planar surface as in Figs. 5b-5c.

As described in the specification at page 10, lines 18-27, the insulative spacer (44) over the vertical layer is a single CVD deposited, etch resistant oxide film, separate and distinct from the oxide or oxi/nitride isolation layer (68) CVD-deposited over the gate electrode in the first trench as described at page 12, lines 1-11. The composition and thickness of the vertically-oriented insulative layer (44) alone controls the crucial dimension between first and second trench and ultimate packing density of a recessed gate MOS device.

The method and resulting structure of Figs. 2c-2d in Sakamoto has the disadvantage that the dimensional control of the sidewall spacer (13) is determined by two steps,

polysilicon local oxidation (9) and deposition and etch of sidewall patch-up (13). Depending on the thermal oxide (9) thickness grown from the polysilicon gate (8), the re-entrant lower portion of the sidewall of (9) is difficult to be filled completely leading to an electrically and mechanically weak spacer. As we push for higher packing density in moving toward thinner and thinner spacer width, the Sakamoto structure poses a serious weakness.

The method and structure of Fig. 5b of Sakamoto has similar problems, 1) the undercut etch uniformity is difficult to control over a large area, and 2) the same problem of a deposited films to fill the "undercut" area reliably. There will be "voids" in the undercut region depending on extent of the undercut. In the subsequent planarizing etch back in Fig. 5c, this weakness is exposed leading to imperfect masking for the second trench etch and defective isolation of source conductor (15) to the gate conductor (8).

The invention as recited in claim 40 includes high quality deposited sidewall spacer (vertically-oriented insulative layer), well-controlled in thickness and composition in combination with a deposited isolation layer. This structure ensures the highest insulative property between gate and source conductors along the sidewall spacers and uniform, dimensional control between first and second trench. Accordingly, claims 40-42 should be allowable.

Applicant traverses the rejection of claims 23, 31, 32, 34-36 and 39 on Sakamoto and Davies as being obvious. The Examiner considers Sakamoto to have all the features of the claim except a p+ doping in the bottom of the second trench to enhance avalanche resistance. Davies teaches a p+ layer in the bottom of the trench to reduce gain and base resistance of the parasitic bipolar transistor turn on, thus extending the safe operating area of the transistor.

At the end of page 3 of the Action, the Examiner makes the remarks about it being "obvious" for the vertically-oriented layer to have a lateral thickness of less than one micron (and less than 0.5 um) because it "depends on the size of the device." Why is it obvious?

The "size" of the device has no bearing on the dimension of the sidewall spacer, or vice versa. The size of a device of this type ordinarily refers to die size. Size can also refer to its current-carrying capacity, which is a function of total gate width. Neither of these parameters relate in any meaningful way to the thickness of the sidewall spacer, or the thickness of the vertical portion of the substrate.

The advantage of the invention not mentioned in the Action is that making the vertically-oriented layer thin provides the highest packing density with this technology and doing so with a thin sidewall spacer provides the best lateral isolation between gate and source with ensured manufacturing control.

Page 3, line 27, of the specification refers to cell density, i.e., 2um/2um in source/gate dimensions. Following this dimension, Fig. 3 regions (40) and (42) will each be 2 um across. If a 0.5 um spacer (44) is formed on either side of block (40), as shown in Fig. 4, the opening (50) will be 1 um in dimension at most. After the gate oxide layer (66) is formed at Fig. 6 is about 500 Å (.05 um) and the second trench (80) is formed, the thickness (88) is less than .5 um.

In view of the foregoing amendments and remarks, the application should be in condition for allowance. If any questions remain, the Examiner is requested to call the undersigned.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

By _____
Alexander C. Johnson, Jr.
Registration No. 29,396

1030 S.W. Morrison Street
Portland, Oregon 97205
Telephone: (503) 222-3613